IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	:	**Mail Stop Appeal Brief - Patents**
Du-Yeul KIM	:	Group Art Unit: 2185
Application No. 10/824,401	:	Examiner: Arpan P. SAVLA
Filed: April 15, 2004	:	

PIPELINE MEMORY DEVICE EMPLOYING A DATA FETCHING METHOD THAT CAN BE OPERATED AT HIGHER FREQUENCIES

APPELLANT'S BRIEF

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

In connection with the above-identified application, please enter this Appellant's Brief in support of Applicant's appeal before the Board of Patent Appeals and Interferences.

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REAL PARTY IN INTEREST

The real party in interest is the assignee of record of the application, namely, Samsung Electronics Co., Ltd., located at 416, Maetan-dong, Yeongtong-gu, Swon-si, Gyeonggi-do, Korea.

RELATED APPEALS AND INTERFERENCES

There are no prior or pending appeals, judicial proceedings or interferences known to the Appellant which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-16 are pending in the application.

Claims 1-3 and 6-16 stand finally rejected.

Claims 4-5 are allowable but stand rejected as being dependent upon a rejected base claim.

Claims 1-3 and 6-16 are the claims appealed.

STATUS OF AMENDMENTS

An Amendment After Final was filed on November 22, 2006. This Amendment was entered by the Examiner to place the Application in a better form for appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

General

The invention of the appealed claims is generally directed to fetching data from a semiconductor memory device. As is well known, most electronic systems include a number of semiconductor memory devices that are used to store data. Furthermore, there is now a growing requirement that these semiconductor memory devices store a large amount of data and operate at higher speeds than before.

Conventional semiconductor memory devices include a pipeline memory system that is used to store and retrieve data in the memory device. See, for example, the "Description of the Related Art" portion of the Specification (page 1, lines 15-35) and FIG. 1 which discuss a conventional pipeline memory system. Specifically, a conventional pipeline memory system uses first through third pipeline stages to output data. See Specification page 2, lines 5-9. Furthermore, the first through third pipeline stages output data in response to a first pipeline control signal (FRP), a second pipeline control signal (SRP), and a data output clock signal (CLKDQ), respectively. See id. and FIG. 1.

However, as described on page 3, lines 1-5 of the Specification, conventional pipeline memory systems use control circuits that generate the FRP and SRP independent of each other. This may lead to problems, especially when the semiconductor memory device is operated at high frequencies. For example, as described in the Specification at page 2, lines 21-35, while outputting data of memory cells, a time margin $\Delta T1$ is required between the point at which FRP is activated and the point at which SRP is deactivated. Furthermore, the FRP and the SRP cannot overlap in time while they are active. Because the conventional pipeline system generates the FRP and SRP independent of each other, the time margin $\Delta T1$ cannot be controlled based on the operating frequency of the device. This may limit the operation of the conventional pipeline system, especially at high frequencies. Thus, one objective of the invention is

to generate the FRP and SRP in a manner such that the time margin ΔT1 can be varied based on the operating frequency of the memory device. According to some embodiments of the invention, the SRP is generated based on the FRP and an additional clock signal, such that the time margin ΔT1 can be controlled based on the operating frequency of the semiconductor device.

Independent Claim 1

Claim 1 is an apparatus claim. A portion of the subject matter of this appealed claim is generally described in the "Description of the Related Art" section of the Specification and the inventive subject matter of this claim is described in the "Detailed Description of the Invention" portion of the Specification.

> *"a data fetching control circuit that is configured to generate:*
> *a first pipeline control signal, in response to a first clock signal for generating the first pipeline control signal"*

Claim 1 is directed, among other things, towards a data fetching control circuit. In an exemplary embodiment, the control circuit generates a first pipeline control signal (FRP) in response to a clock signal. See, for example, FIGs 1 and 6 and accompanying text. However, in addition to the above-claimed subject matter, claim 1 also includes:

> *"a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal."*

Thus, claim 1 also includes a claim feature directed towards a data fetching control circuit that generates a second pipeline control signal (SRP) in response to two signals: (1) a second clock signal and (2) the first pipeline signal. See for example, page 5, lines 5-33 and page 6, lines 1-14 of the Specification. In addition, Figures 5 and 6 disclose alternative exemplary embodiments that are covered by the above-discussed

subject matter of claim 1.

Independent Claim 6

Claim 6 is a method claim that includes claim features similar to claim 1. Namely claim 6 includes:

> "*generating a first pipeline control signal in response to a first clock signal for generating a first pipeline control signal;*
> *generating a second pipeline control signal in response to a second clock signal for generating a second pipeline control signal and the first pipeline control signal;*"

The above-claimed subject matter is similar to that discussed with respect to claim 1 and is also described in the text and figures of the Application referred to in the discussion of claim 1.

Independent Claim 9

Claim 9 is an apparatus claim that has a scope different than that of claim 1. In particular, claim 9 includes a combination of elements including, *inter alia*:

> *"a first pipeline stage coupled to the output of the at least one memory cell, wherein the first pipeline stage is driven by a first control signal; and*
> *a second pipeline stage coupled to the output of the first pipeline stage, wherein the second pipeline stage is driven by the first control signal and a second control signal."*

Thus, claim 9 recites a first pipeline stage that is driven by a first control signal and a second pipeline stage that, unlike the conventional pipeline stage that is driven by only a second control signal, is driven by two signals: (1) the first control signal and (2)

a second control signal. See, for example, FIG 4; and page 5, lines 15 to 21, of the Specification.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection presented for review are as follows:

1. Whether claims 1 and 6-14 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Applicant's "Description of the Related Art" ("DRA") in view of Lee (U.S. Patent No. 6,564,287);
2. Whether claims 2-3 and 15 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Applicant's DRA in view of Lee and Paul et al. ("Paul") (U.S. Patent No. 6,629,226); and
3. Whether claim 16 is unpatentable under 35 U.S.C. § 103(a) as being obvious over Applicant's DRA in view of Lee and Shinozaki (U.S. Patent No. 6,084,802.)

ARGUMENT

I. GENERAL OBSERVATIONS

The Appellant has carefully considered the Examiner's comments contained in the Office Action dated October 6, 2006, and in the Advisory Action dated December 19, 2006. As discussed in detail below, the Appellant contends that that the Examiner is unreasonably interpreting the claims of the Application – so much so that the Examiner has vitiated the plain meaning of the claims. Further, as also discussed in detail below, Appellant contends that the Examiner has failed to properly consider the teachings of the references as a whole, and has relied on hindsight reconstruction of the references in a rather tortured attempt to "force" the references read on the appealed claims.

II. CLAIMS 1 AND 6-14 ARE ALL PATENTABLE OVER APPELLANT'S DRA IN VIEW OF LEE.

Claims 1 and 6-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's "Description of the Related Art" ("DRA") in view of Lee (U.S. Patent No. 6,564,287).

As discussed in detail below, Appellant makes two separate and independent arguments to traverse this rejection, namely:

(1) The rejected claims define over the cited references even if the references are somehow combined as suggested by the Examiner, and

(2) One of ordinary skill in the art would not combine the teachings of the cited references in the fashion suggested by the Examiner.

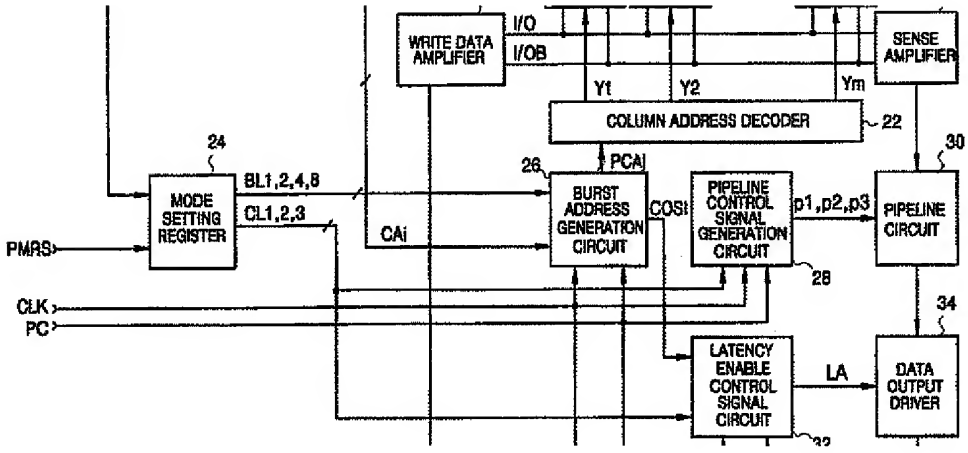
Claim 1

Claim 1 is patentable over the combination of Appellant's DRA and Lee.

Lee is generally directed towards a semiconductor device in which the burst

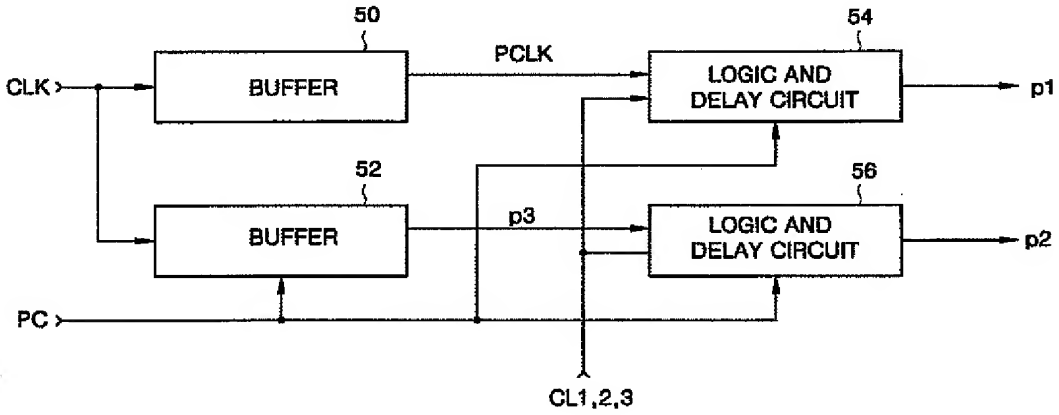
length and/or a column address strobe (CAS) latency is fixed. To this end, Lee discloses a block diagram of conventional semiconductor device as shown in FIG. 1, a portion of which is illustrated below.

FIG. 1
(PRIOR ART)



Specifically, the prior art device shown in FIG. 1 includes a pipeline control signal generation circuit 28 that the Examiner **incorrectly contends** as reading on the subject matter of claim 1. Lee describes the pipeline control signal generation circuit 28 in FIG. 3 as illustrated on the next page.

FIG.3
(PRIOR ART)



The Examiner fairly admits that Applicant's DRA did not disclose the following claim features of claim 1:

> *"a data fetching control circuit that is configured to generate:*
>
> *a first pipeline control signal, in response to a first clock signal for generating the first pipeline control signal"*
> *"a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal."*

However, the Examiner then attempts to "force" the pipeline control signal generation circuit 28 of FIG. 3 to read on the above-claimed subject matter. No reasonable interpretation of FIG. 3 can possibly read on these claim recitations. In particular, the circuit of FIG. 3 in Lee is not configured to generate

> "*a second pipeline control signal, in response to* ***both a second clock signal*** *for generating the second pipeline control signal* ***and the first pipeline control signal.***" (Emphasis added.)

In an attempt to get around this clear omission in Lee, the Examiner becomes quite creative in his rejection.

That is, the Examiner characterizes element p3 in FIG. 3 as a "first pipeline control signal" and clock signal CLK in FIG. 3 as a "first clock signal." In addition, the Examiner characterizes element p2 in FIG. 3 as a "second pipeline control signal". Then, knowing that "logic and delay circuit 56" in FIG. 3 is driven by only one control signal p3 (and **not** by any clock signal), the Examiner proceeds to interpret control signal p3 as **both** a control signal **and** a clock signal. See Office Action of October 6, 2007, pages 4-5.

This is clearly an unreasonable interpretation of the appealed claims and Lee..

More precisely, Appellant submits that such an **interpretation of element p3 as both a control signal and clock signal is completely unreasonable.** To this end, Appellant makes reference to § 2111 of the M.P.E.P:

> During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." (Emphasis added.) M.P.E.P. § 2111 8th ed. Rev. 5

Furthermore, the M.P.E.P also states:

> The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. Id. (Emphasis added.)

In response, in the Advisory Action of record, the Examiner states:

> *"[c]laim 1 was given its broadest reasonable interpretation consistent with the specification. However, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. Thus, it is noted that the features upon which Applicants relies (i.e., the presence of two separate signals) are not recited in the rejected claim."* See Advisory Action, Continuation Sheet. (Internal citations omitted.)

It is clear that the Examiner has misunderstood Appellant's argument.

Specifically, Appellant is **not** importing limitations from the Specification into the claims. Rather, Appellant is interpreting the claims as a person having ordinary skill in the art would, **without** referring to the Specification.

Indeed, Appellant submits that, on their face, the claim recitations "a second clock signal" and "a first pipeline control signal" would clearly be reasonably interpreted as **two separate signals** – no importation of limitations from the specification is needed to reach this interpretation.

Again, it is clear from the Office Action and the Advisory Action that the Examiner is trying to interpret signal p3 of Lee as **both** a control signal **and** a clock signal in an attempt to make Lee read on claim features of claim 1. One having ordinary skill in the art would not reasonably interpret "a second clock signal" and "a first pipeline control signal" as a single signal, and it is clear that the combination of Applicant's DRA and Lee fails to disclose each and every element of the appealed claims.

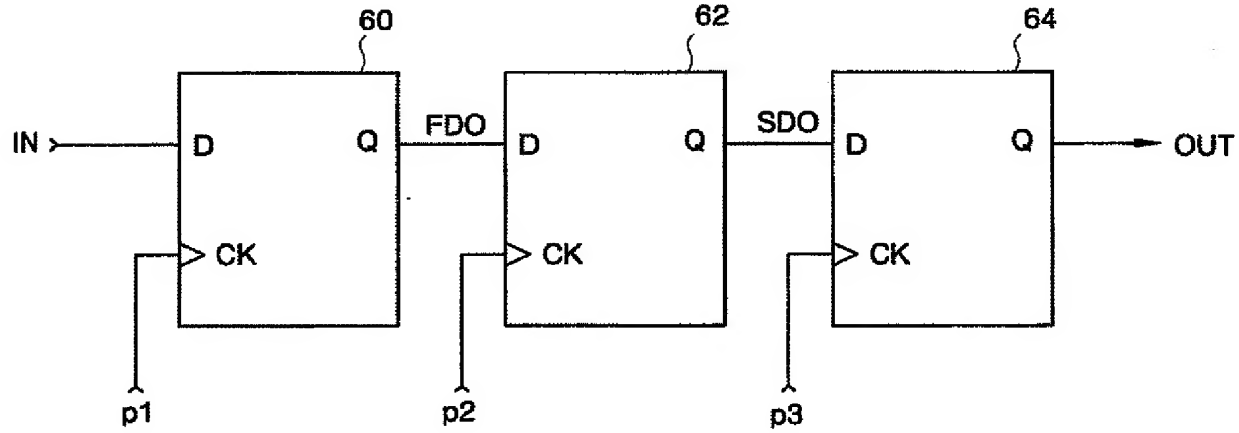
Therefore, for at least the reasons discussed above, claim 1 defines over the

combination of Applicant's DRA and Lee, even if Applicant's DRA and Lee are somehow combined as suggested by the Examiner.

Moreover, Appellant respectfully contends that one having ordinary skill in the art would not combine the teachings of the cited references in the fashion suggested by the Examiner.

FIG. 1 of Lee discloses a pipeline signal generation circuit 28 that is connected to a pipeline circuit 30. See portion of FIG. 1 of Lee in present Brief at page 13. Figure 4 of Lee, as shown below discloses an embodiment of pipeline circuit 30.

FIG.4
(PRIOR ART)



As seen above, Lee discloses three D flip flops 60. 62. and 64. Furthermore, signal p1 drives flip flop 60, p2 drives flip flop 62, and p3 drives flip flop 64. Now, interpreting FIG. 3 in light of FIG. 4, the Board will appreciate that signal p3 (that is equated to a "first pipeline control signal" by the Examiner) drives the **third** flip flop 64. That is, a **first pipeline control signal** drives the **third stage** of the pipeline control circuit 30. In light of this, the Board will also appreciate that a first pipeline control signal driving a

third stage does not constitute "**a first pipeline stage** that latches the data on the data transfer path in response to the **first pipeline control signal**" or "**a third pipeline stage** that outputs the data latched by the second pipeline stage to a data output pad in response to a **data output clock signal**," as required by claim 1. (Emphasis added.)

Thus, unlike the claim recitation in claim 1, signal p3 in Lee is used to control a **third** pipeline stage 64 and **not** a first pipeline stage 60. This goes against the teachings of claim 1. Therefore, this disclosure in Lee would not result in one of ordinary skill in the art to combine Lee with Appellant's DRA to produce the claim recitations of claim 1. Indeed, in order to combine Lee with Appellant's DRA, one having ordinary skill in the art would have to **completely reconfigure** the circuit in Lee so as to feed data from pipeline stage 64 to pipeline stage 62, something that is **not** taught or suggested by any portion of Lee. Thus, nothing in Appellant's DRA or Lee, when considered in its entirety, provides a motivation or suggestion to combine the two to produce the claim recitations of claim 1.

When this issue was brought to the attention of the Examiner, the Examiner responded in the Advisory Action stating:

> *"[The Examiner] asserts that the Lee reference has been considered in its entirety, although the Examiner still maintains that is it the teaching of FIG. 3 in Lee (i.e., the pipeline control generation circuit) that is used in combination with Applicant's DRA."* See Advisory Action Continuation Sheet, paragraph 2.

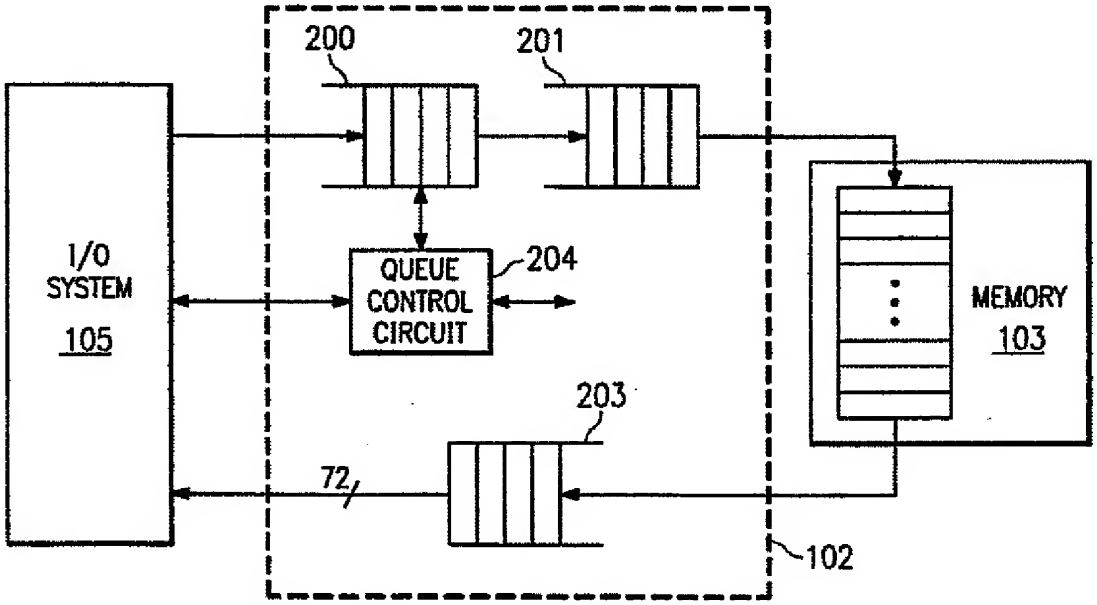
This argument is flawed for a number of reasons. First, the Examiner asserts the consideration of Lee in its entirety without addressing Appellant's argument regarding the teaching in FIG. 4. Second, in the same breath, the Examiner asserts that it is **only** the teaching of FIG. 3 that is considered. (Emphasis added.) These two statements contradict each other. Just picking and choosing a portion of a reference to suit the Examiner's needs cannot, and indeed does not, constitute considering a prior art

reference in its entirety. As already discussed above, one skilled in the art will not consider FIG. 3 of Lee in isolation without regard to FIG. 4 as both the figures are part of the **same** embodiment in Lee. Thus, for at least the reasons discussed above, Appellant submits that the motivation or suggestion to combine is not provided in Applicant's DRA and Lee. It therefore follows that the teachings of the prior art do not provide a reasons to combine the references cited by the Examiner.

In the alternative, the Examiner also maintains that "Adkisson (U.S. Patent No. 5,590,304) states [that] the burst length and burst frequency are programmable providing operational flexibility." See Office Action dated October 6, 2006, page 14 (citing Adkisson column 6, lines 3-5.) (Internal quotations omitted.) This, in view of the Examiner, proves that the motivation to combine Applicant's DRA and Lee was available generally to one having ordinary skill in the art. However, in making this assertion, the Examiner has misunderstood and/or misapplied the Adkisson reference.

Adkisson is directed towards systems and methods for preventing queue overflows in data processing systems. See, for example, FIG. 2 from Adkisson that is reproduced on the next page.

FIG. 2



In particular, FIG. 2 includes an I/O system 105 that sends and receives memory requests to memory 103 through an input queue 200, a cross bar queue 201, and through a return queue 203. See Adkisson column 5, lines 25-55. Adkisson discloses that Queue control 204 is conditioned to prevent overflows in the queues by controlling the maximum size of the bursts of memory requests from I/O system 105 and queues 200 and 201 to memory 103. See Adkisson column 6, lines 40-43. Furthermore, the Queue control circuitry 204 also controls the wait time between bursts of memory requests from queue 200 so that queue 203 has sufficient time to empty between the resulting bursts of data from memory 103. See Adkisson column 6, lines 57-62. Thus, Adkisson tries to solve the problem of queue overflow by controlling the burst size and burst frequency of memory requests by using a queue control circuit 204.

It is unclear how controlling the burst length and frequency of **memory requests** in a **queuing system** is related to controlling the generation of **control signals** that are used to **output data from a pipeline circuit to an external system.** Indeed, knowing

that the burst frequency and burst size of memory requests is adjustable does not provide one skilled in the art the motivation to control the generation of control signals (not memory requests) that are used to output data to an external system in a controlled manner.

Finally, the nature of the problem to be solved does not provide a motivation to combine the references. For example, Lee is directed towards a semiconductor device having a fixed latency operation mode and/or a fixed burst operation mode. See Lee column 1, lines 5-10. Specifically, Lee discloses that a latency operation refers to a column address strobe latency operation, which is a time delay between the time the data is output and the time a read signal is applied. See Lee column 1, lines 17-20. Also, a burst operation in Lee refers to a situation when a column address is input after a row address is input and, thereafter, data from the column addresses is output at high speed in synchronization with a clock signal. See Lee column 1, lines 37-40. None of these objectives are even remotely related to controlling the generation of pipeline control signals as required by claim 1.

Indeed, Appellant's contention is reinforced by the explicit disclosure in Lee which states that **only** the **mode setting register 24** and the **burst address generation circuit 26** of the prior art semiconductor device shown in FIG. 1 of Lee is varied by the disclosed embodiment in Lee. See Lee column 7 lines 65-67; and column 8 lines 1-7. That is, the pipeline control signal generation circuit 28 and the pipeline circuit 30 (the two circuits that allegedly read on the claim recitations of claim 1) are not even part of the invention in Lee.

On a final note with respect to claim 1, the Examiner also asserted that "feeding an output of Lee's pipeline control signal generation circuit into a stage of Applicant's DRA pipeline memory device would constitute a reasonable expectation of success." See Advisory Action Continuation Sheet, paragraph 2. Appellant disagrees with this assertion, which is entirely unsupported by the evidence on record. Respectfully, Appellant also contends the statement is clear

indicia of hindsight reconstruction of the references.

Claim 6

Independent claim 6 is a method claim that includes elements similar to that of claim 1. For example, independent claim 6 includes a combination of claim recitations including, *inter alia*:

> "*generating a first pipeline control signal in response to a first clock signal for generating a first pipeline control signal;*
> *generating a second pipeline control signal in response to a second clock signal for generating a second pipeline control signal and the first pipeline control signal.*"

The comments presented above regarding independent claim 1 are equally applicable to independent claim 6. As such, reference is made to those previous comments. Moreover, Appellant submits that claim 6 is allowable over the combination of Appellant's DRA and Lee at least in light of the comments made regarding independent claim 1.

Claim 9

Claim 9 is an apparatus includes a combination of claim recitations including *inter alia*:

> *"a first pipeline stage coupled to the output of the at least one memory cell, wherein the first pipeline stage is driven by a first control signal; and*
> *a second pipeline stage coupled to the output of the first pipeline stage, wherein the second pipeline stage is driven by the first control signal and a second control*

signal"

No combination of Appellant's DRA and Lee could produce an apparatus including such a combination of claim recitations.

The Examiner fairly admits that Appellant's DRA does not expressly disclose the second pipeline stage driven by the first control signal and a second control signal. See Office Action dated October 6, 2006, page 8. Instead, the Examiner asserts that Lee discloses a second control signal driven by a first control signal. See id. (citing Lee column 3, lines 34-37; FIG. 3, elements 56, p2, and p3.)

While apparently, Lee discloses a second control signal p2 being driven by a first control signal, Appellant simply does not understand how a **second control signal p2 being driven by a first control signal** constitutes "a second pipeline stage coupled to the output of the first pipeline stage, wherein the **second pipeline stage is driven by the first control signal and a second control signal.**" Indeed, assuming *arguendo*, that the logic and delay circuit 56 of Lee is analogous to a "second pipeline stage," the Examiner's assertion falls flat on its face because circuit 56 is **not** driven by both signal p2 and p3. Instead, as is explicitly shown in FIG. 3 of Lee, circuit 56 is **driven by signal p3 to output p2.**

Later in prosecution, the Examiner seemingly backtracks and states the following in the Advisory Action:

> *"[T]he Examiner has not relied on Lee for the teaching of the second pipeline stage. The Examiner relies on the second pipeline stage of Applicant's DRA (Fig.1, element 28) in combination with Lee's pipeline control signal p3 and p2."*

The Examiner has again overlooked a fundamental tenet of patent law, namely,

"A prior art reference must be considered in its entirety, i.e.,

as a whole, including portions that would lead away from the claimed invention." M.P.E.P. § 2141.02-VI 8th ed., Rev. 5

Reading FIG. 3 in light of FIG. 4 of Lee, which is part of the **same** embodiment that includes FIG. 3, it is evident that signal p3 is used to drive a third stage and signal p2 is used to drive a second stage. Nothing in Lee or in the other prior art cited even remotely suggests taking the two control signals from Lee and using these signals to drive the second pipeline stage in Appellant's DRA. To this end, reference is made to the comments made regarding the rejection of claim 1 with respect to the Examiner's alleged motivation to combine Lee and Appellant's DRA.

No reasonable combination of Appellant's DRA and Lee could produce the apparatus of claim 9.

Claims 10-14

Dependent claims 10-14 depend from independent claim 9 and include additional recitations of novelty. Furthermore, the Appellant does not acquiesce that the rejections of dependent claims 10-14 stand and fall together with the rejection of independent claims 1, 6, and 9. However, because the rejection of independent claims 1, 6, and 9 are clearly without merit, and for the sake of brevity, the rejection of these dependent claims is not separately argued with respect to their Section 103 rejection over Appellant's DRA and Lee.

III. CLAIMS 2-3 AND 15 ARE ALL PATENTABLE OVER APPELLANT'S DRA IN VIEW OF LEE AND PAUL ET AL.

Claims 2-3 and 15 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Appellant's DRA in view of Lee and Paul et al. ("Paul") (U.S. Patent No.

6,629,226.)

Claims 2-3 and 15 ultimately depend from one of independent claims 1 and 9 and include additional recitations of novelty. The Appellant does not acquiesce that the rejections of dependent claims 2-3 and 15 stand and fall together with the rejection of independent claims 1 and 9. However, because the rejections of independent claims 1 and 9 are clearly without merit based on the discussion above, and for the sake of brevity, the rejection of these dependent claims is not separately argued with respect to their Section 103 rejection over Appellant's DRA in view of Lee and Paul.

IV. CLAIM 16 IS PATENTABLE OVER APPELLANT'S DRA IN VIEW OF LEE AND SHINOZAKI (U.S. PATENT NO. 6,084,802)

Claim 16 depends from claim 9 and includes additional recitations of novelty. The Appellant does not acquiesce that the rejections of dependent claim 16 stands and falls together with the rejection of independent claim 9. However, because the rejection of independent claim 9 is clearly without merit based on the discussion above, and for the sake of brevity, the rejection of this dependent claim is not separately argued with respect to its Section 103 rejection over Appellant's DRA in view of Lee and Shinozaki.

V. CONCLUSION

For at least the reasons given herein, Appellant respectfully contends that (a) the Examiner has not established a *prima facie* case of obviousness with respect to the subject matter defined by the appealed claims, and (b) the subject matter of the appealed claims would not have been obvious to one of ordinary skill in view of the teachings of the cited references.

Respectfully submitted,

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CLAIMS APPENDIX

1. A pipeline memory device comprising:

a plurality of memory cells that store data;

a data transfer path on which the data is transferred;

a data fetching control circuit that is configured to generate:

a first pipeline control signal, in response to a first clock signal for generating the first pipeline control signal: and

a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal;

a first pipeline stage that latches the data on the data transfer path in response to the first pipeline control signal;

a second pipeline stage that latches the data latched by the first pipeline stage in response to the second pipeline control signal; and

a third pipeline stage that outputs the data latched by the second pipeline stage to a data output pad in response to a data output clock signal.

2. The pipeline memory device of claim 1, wherein the data fetching control circuit comprises:

a first edge trigger delay circuit that receives the first clock signal for generating the first pipeline control signal and generates the first pipeline control signa l; and

a multiplexer that receives the second clock signal for generating the second pipeline control signal and the first pipeline control signal, and generates the second pipeline control signal.

3. The pipeline memory device of claim 2, wherein the first edge trigger delay circuit comprises an even number of inverters in a chain.

6. A data fetching method for a pipeline memory device, comprising:

transferring data stored in memory cells along a transfer path;

generating a first pipeline control signal in response to a first clock signal for generating a first pipeline control signal;

generating a second pipeline control signal in response to a second clock signal for generating a second pipeline control signal and the first pipeline control signal;

latching the data to a first pipeline stage on the transfer path in response to the first pipeline control signal;

latching the data to a second pipeline stage on the transfer path in response to the second pipeline control signal; and

outputting the data from the second pipeline stage to a data output pad in response to a data output clock signal.

7. The method of claim 5, wherein a point of activation of the second pipeline control signal is determined depending on a point of activation of the first pipeline control signal.

8. The method of claim 5, wherein the second pipeline control signal is activated when the first pipeline control signal is inactive.

9. An apparatus comprising:

at least one memory cell;

a first pipeline stage coupled to the output of the at least one memory cell, wherein the first pipeline stage is driven by a first control signal; and

a second pipeline stage coupled to the output of the first pipeline stage, wherein

the second pipeline stage is driven by the first control signal and a second control signal.

10. The apparatus of claim 9, wherein the first control signal and the second control signal are driven by a clock signal.

11. The apparatus of claim 10, wherein the clock signal is an internal clock signal.

12. The apparatus of claim 10, wherein:
the first control signal is delayed from the clock signal by a first delay; and
the second control signal is delayed from the clock signal by a second delay.

13. The apparatus of claim 12, wherein the first delay is larger than the second delay.

14. The apparatus of claim 9, wherein the first control signal and the second control signal are never in an active state at the same time.

15. The apparatus of claim 9, wherein the second pipeline stage is driven by the first control signal, and the second control signal utilizes a multiplexer.

16. The apparatus of claim 9, wherein the second pipeline stage is driven by the first control signal, and the second control signal utilizes a NAND gate.

EVIDENCE APPENDIX

[There is no evidence to be attached to this Brief]

RELATED PROCEEDINGS APPENDIX

[There are no related proceedings.]